IN THE UNITED STATES PATENT OFFICE

Applicant:	Stephen M. Douglass et al.
Assignee:	Xilinx, Inc.
Title:	Method and Apparatus for Processing Data Within a Programmable Gate Array Using Fixed and Programmable Processors

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PRELIMINARY AMENDMENT

Before taking action in the above-referenced case, please make the following amendments to the claims.

IN THE CLAIMS

Please add Claims 39-43 as follows:

39. (New) A system, comprising:

a memory device; and

a field programmable gate array, wherein the field programmable gate array comprises:

a logic fabric that includes a plurality of configurable logic blocks, switching blocks, and input/output blocks, wherein at least a portion of the logic fabric is configured as a first configured processor to perform a first fixed logic function, and at least a portion of the input/output blocks are coupled to the memory device;

a fixed logic processor embedded within the logic fabric; and

a first auxiliary processing interface that couples the first configured processor to perform the first fixed logic function to the fixed logic processor.